Amendments to the Specification:

Please replace paragraph the paragraph beginning at page 5, line 12 with the following amended paragraph:

The above-described object is also achieved by a semiconductor memory device comprising: a silicon layer having a first diffused region and a second diffused region formed therein; a gate electrode formed through an insulating film on one side of the silicon layer between the first and the second diffused regions; a capacitor formed on said one side of the silicon layer and having a storage electrode connected to the first diffused region; a bit line formed on said one side of the silicon layer and connected to the second diffused region; and a ~~scrapping~~ strapping word line formed on the other side of the silicon layer and connected to the gate electrode, whereby a semiconductor memory device of SOI structure can be easily fabricated.

Please replace paragraph the paragraph beginning at page 8, line 10 with the following amended paragraph:

In the above-described semiconductor memory device it is preferable that the semiconductor memory device further comprises a ~~scrapping~~ strapping word line formed on said other side of the semiconductor layer and connected to the gate electrode, whereby the ~~scrapping~~ strapping word line can be easily formed without restriction by the structure of the capacitor, etc.

Please replace paragraph the paragraph beginning at page 8, line 17 with the following amended paragraph:

In the above-described semiconductor memory device it is preferable that the semiconductor memory device further comprises a ~~scrapping~~ strapping word line formed on said one side of the semiconductor layer and connected to the gate electrode.

Please replace paragraph the paragraph beginning at page 11, line 25 with the following amended paragraph:

In the above-described method for fabricating the semiconductor memory device, it is preferable that the method further comprises, after the semiconductor layer forming step, a ~~scrapping~~ strapping word line forming step of forming a ~~scrapping~~ strapping word line connected to the gate electrode.

Please replace paragraph the paragraph beginning at page 12, line 4 with the following amended paragraph:

In the above-described method for fabricating the semiconductor memory device, it is preferable that the method further comprises, after the diffused region forming step, a ~~scrapping~~ strapping word line forming step of forming a ~~scrapping~~ strapping word line connected to the gate electrode.

Please replace paragraph the paragraph beginning at page 14, line 8 with the following amended paragraph:

In the above-described method for fabricating the semiconductor memory device it is preferable that the method further comprises, the method further comprises, before the gate

electrode forming step, a device isolation film forming step of forming on said one side of the w semiconductor substrate a device isolation film which defines a device region, and a opening forming step of removing the device isolation film in the first region of the device isolation film to form an opening; the method further comprises, after the semiconductor layer forming step, a ~~scrapping~~ strapping word line forming step of forming a ~~scrapping~~ strapping word line connected to the gate electrode; in the gate electrode forming step the gate electrode extended in the first region is formed buried in the opening; and in the ~~scrapping~~ strapping word line forming step the ~~scrapping~~ strapping word line is connected with the gate electrode in the first region, whereby the gate electrodes and the ~~scrapping~~ strapping word lines can be easily connected with each other.

Please replace paragraph the paragraph beginning at page 19, line 23 with the following amended paragraph:

FIG. 34 is a diagrammatic sectional view of the semiconductor memory device of FIG. [[23]] 32 along the B-B' part.

Please replace paragraph the paragraph beginning at page 22, line 1 with the following amended paragraph:

A ~~scrapping~~ strapping word line 46 for decreasing electric resistance of the word line is formed on the bit lines 42 through an insulating film 44. The ~~scrapping~~ strapping word lines 46 are connected to the gate electrodes 18 at a certain pitch in a region between the cell arrays and function to supplement the gate electrodes 18, whose resistance is difficult to decrease. That is,

voltage decrease of the gate electrodes 18 due to resistance increase of the gate electrodes 18 due to micronization, etc. is prevented.

Please replace paragraph the paragraph beginning at page 28, line 22 with the following amended paragraph:

In the present embodiment, the bit lines 42 are formed after the capacitors are formed, and no high-temperature heat treatment is necessary after the formation of the bit lines 42. The bit lines 42 are formed of a low-resistance metal material, such as aluminium, Ti (titanium), TiN (titanium nitride), W (tungsten) or others, and can have a thickness of below about 1/10 the thickness of the bit lines formed of a high-melting point material, such as polycrystal silicon, tungsten silicide or others. By making the thickness of the bit lines small, a step on the bit lines 42 can be made extremely small. Accordingly, in forming, e.g., the ~~scrapping~~ strapping word lines 46 above the bit lines 42, no planarization is necessary, or the planarization step can be simplified.

Please replace paragraph the paragraph beginning at page 29, line 10 with the following amended paragraph:

Then, the ~~scrapping~~ strapping word lines 46 are formed on the bit lines 42 through the insulating film 44 (FIG. 4B).

Please replace paragraph the paragraph beginning at page 29, line 12 with the following amended paragraph:

The ~~scrapping~~ strapping word lines 46 can be formed by the fabrication steps exemplified in FIG. 5. FIG. 5 shows sectional views of the device along the word lines.

Please replace paragraph the paragraph beginning at page 29, line 15 with the following amended paragraph:

In the step of FIG. 2B, before the gate oxide film 14 is formed, the device isolation film 12 in regions where the word line contacts are to be formed is etched off. Thus the formed gate electrodes 18 are buried in the ~~scrapping~~ strapping word line contacts (FIG. 5A).

Please replace paragraph the paragraph beginning at page 29, line 20 with the following amended paragraph:

Then, in the step of FIG. 4B, when the bit lines 42 are formed, a wiring material 48 is formed on the gate electrodes 18 of the ~~scrapping~~ strapping word line contacts (FIG. 5B).

Please replace paragraph the paragraph beginning at page 29, line 24 with the following amended paragraph:

Subsequently when the ~~scrapping~~ strapping word lines 46 are formed, contact holes for exposing the wiring material 48 are formed in the insulating film 44, and the gate electrodes 18 and the ~~scrapping~~ strapping word lines 46 are connected to each other through the contact holes.

Please replace paragraph the paragraph beginning at page 30, line 3 with the following amended paragraph:

Thus the ~~scrapping~~ strapping word lines 46 are formed.

Please replace paragraph the paragraph beginning at page 30, line 18 with the following amended paragraph:

The capacitors are formed on the side of the support substrate, and the ~~scrapping~~ strapping word lines are formed through the semiconductor layer on the opposite side, whereby the contact holes interconnecting the word lines and the ~~scrapping~~ strapping word lines can be very shallow, and the formation of the contacts can be very simple.

Please replace paragraph the paragraph beginning at page 31, line 7 with the following amended paragraph:

The semiconductor memory device according to the present embodiment includes the ~~scrapping~~ strapping word lines, but as shown in FIG. 6, the ~~scrapping~~ strapping word lines 46 may not be formed.

Please replace paragraph the paragraph beginning at page 31, line 11 with the following amended paragraph:

In the present embodiment, the ~~scrapping~~ strapping word lines 46 are formed above the bit lines 42, but the bit lines 42 may be formed above the ~~scrapping~~ strapping word lines 46.

Please replace paragraph the paragraph beginning at page 32, line 17 with the following amended paragraph:

That is, after the bit lines 42 are formed, the shield electrode 54 is formed through an insulating film 52. Then an insulating film 44 is deposited on the shield electrode 54, and the ~~scrapping~~ strapping word lines 46 are formed as required.

Please replace paragraph the paragraph beginning at page 32, line 25 with the following amended paragraph:

In the case that the shield electrode 54 is provided in the semiconductor memory device according to the present embodiment, the shield electrode 54 is present only in the cell arrays and is absent between the cell arrays. The shield electrode 54 is not a barrier to forming the contacts between the ~~scrapping~~ strapping word lines 46 and the gate electrodes 18 in the regions between the cell arrays.

Please replace paragraph the paragraph beginning at page 35, line 13 with the following amended paragraph:

The semiconductor memory device according to the present embodiment is characterized in that ~~scrapping~~ strapping word lines 46 are formed on the side of a support substrate 40. That is, the ~~scrapping~~ strapping word lines 46 which decrease electric resistance of word lines 18 are formed below a cell plate 34 through an insulating film 52. The ~~scrapping~~ strapping word lines 46 are connected to the gate electrodes, spaced from each other at a certain pitch.

Please replace paragraph the paragraph beginning at page 37, line 1 with the following amended paragraph:

Next, the ~~scrapping~~ strapping word lines 46 are formed through an insulating film 44. Then, a polycrystal silicon oxide film, for example, is deposited on the ~~scrapping~~ strapping word lines 46 to form an insulating film 58, and next the surface is planarized and adhered to the support substrate 40 (FIG. 11A)

Please replace paragraph the paragraph beginning at page 37, line 15 with the following amended paragraph:

In the method for fabricating the semiconductor memory device according to the second embodiment, it is necessary to connect the gate electrodes 18 and the ~~scrapping~~ strapping word lines 46 with each other, and they can be connected with each other by the steps exemplified in FIG. 13.

Please replace paragraph the paragraph beginning at page 37, line 20 with the following amended paragraph:

In the step of FIG. [[11C]] 10C, before the polycrystal silicon film to be the storage nodes 30 is deposited, the silicon oxide film 16 in regions where ~~scrapping~~ strapping word line contacts are to be formed is removed.

Please replace paragraph the paragraph beginning at page 37, line 24 with the following amended paragraph:

Then, the polycrystal silicon film is processed to be the storage nodes 30 while the polycrystal silicon film is left in the regions for the word line contacts to be formed in. Thus a

wiring material 48 connected to the gate electrodes 18 is formed (FIG. 12A). The sectional view of FIG. 12B has a contraction scale different from that of FIG. 12A to make clear the relationship between the memory cell regions and the ~~scrapping~~ strapping word line contacts. The sectional views following FIG. 12B have the same contraction scale as FIG. 12B.

Please replace paragraph the paragraph beginning at page 38, line 20 with the following amended paragraph:

Subsequently openings are formed in the insulating films 64, 52 on the wiring material 48 and then the ~~scrapping~~ strapping word lines 46 are formed. Thus the gate electrodes 18 (word lines) and the ~~scrapping~~ strapping word lines are connected with each other (FIG. 13C).

Please replace paragraph the paragraph beginning at page 38, line 25 with the following amended paragraph:

Then, a silicon oxide film, for example, is deposited on the ~~scrapping~~ strapping word lines 46, and the surface is planarized and adhered to the support substrate 40. And the structure of FIG. 11A is formed.

Please replace paragraph the paragraph beginning at page 39, line 3 with the following amended paragraph:

Thus the ~~scrapping~~ strapping word lines 46 can be formed.

Please replace paragraph the paragraph beginning at page 39, line 9 with the following amended paragraph:

The wiring material 48 for connecting the ~~scrapping~~ strapping word lines 46 is formed concurrently with formation of the storage nodes 30, whereby the contact holes formed in the insulating film 64 can be made shallow. This facilitates formation of the contacts of the ~~scrapping~~ strapping word lines 46 in a case that the ~~scrapping~~ strapping word lines 46 are formed on the side of the support substrate 40.

Please replace paragraph the paragraph beginning at page 42, line 23 with the following amended paragraph:

Subsequently a silicon oxide film, for example, is deposited by CVD to form an insulating film 44, and ~~scrapping~~ strapping word lines 46 are formed on the insulating film 44 (FIG. 17B).

Please replace paragraph the paragraph beginning at page 43, line 1 with the following amended paragraph:

The ~~scrapping~~ strapping word lines 46 can be formed by the steps exemplified in FIG. 18.

Please replace paragraph the paragraph beginning at page 43, line 3 with the following amended paragraph:

First, before formation of the gate electrodes 18, openings are formed in the device isolation film 12 in regions where the gate electrodes 18 and the ~~scrapping~~ strapping word lines are connected to each other so that the gate electrodes 17 are buried in the openings (FIG. 18A). The

openings may be formed simultaneously with formation of the device isolation film 12 or formed by etching in a following step.

Please replace paragraph the paragraph beginning at page 43, line 16 with the following amended paragraph:

Subsequently the ~~scrapping~~ strapping word lines 46 are formed on the insulating film 44 and are connected to the gate electrodes 18 (FIG. 18B).

Please replace paragraph the paragraph beginning at page 43, line 19 with the following amended paragraph:

Thus the ~~scrapping~~ strapping word lines 46 are formed.

Please replace paragraph the paragraph beginning at page 44, line 1 with the following amended paragraph:

The semiconductor memory device according to the present embodiments include the ~~scrapping~~ strapping word lines 46 but, as shown in FIG. 9, may not include the ~~scrapping~~ strapping word lines 46.

Please replace paragraph the paragraph beginning at page 45, line 11 with the following amended paragraph:

The semiconductor memory device according to the present embodiment is characterized in that the semiconductor memory device according to the third embodiment includes ~~scrapping~~ strapping word lines 46 formed on the side of a support substrate 40.

Please replace paragraph the paragraph beginning at page 45, line 16 with the following amended paragraph:

That is, bit lines 42 are connected to a source diffused region 22 of memory cell transistors on the side of a semiconductor layer 36 which is nearer to a support substrate 40. ~~Scrapping~~ Strapping word lines 46 for decreasing electric resistances of word lines are formed below a cell plate 34 through an insulating film 52. The ~~scrapping~~ strapping word lines 46 are connected to gate electrodes 18 at a certain pitch (FIG. 21).

Please replace paragraph the paragraph beginning at page 46, line 14 with the following amended paragraph:

Then, the ~~scrapping~~ strapping word lines 46 are formed through the insulating film 52.

Please replace paragraph the paragraph beginning at page 46, line 16 with the following amended paragraph:

Next, a silicon oxide film, for example, is deposited on the ~~scrapping~~ strapping word lines 46 to form an insulating film 58, and the surface of the insulating film 58 is planarized (FIG. 22B). The ~~scrapping~~ strapping word lines 46 can be connected to the gate electrodes 18 by the same steps

as those of the method for fabricating the semiconductor memory device according to the second embodiment, which are shown in FIGS. 13 and 14.

Please replace paragraph the paragraph beginning at page 47, line 11 with the following amended paragraph:

As described above, according to the present embodiment, the planarization step in the ~~boded~~ bonded SOI technique and the planarization step in the DRAM fabrication process can be rationalized, whereby even in the case that, the bit lines 42 and the ~~scrapping~~ strapping word lines 46 are formed on the side of the semiconductor layer 36 which is nearer to the support substrate 40, fabrication costs can be much decreased.

Please replace paragraph the paragraph beginning at page 48, line 26 with the following amended paragraph:

On the device layer 50 adhered to the support substrate 40 bit lines 42 connected to the source diffused region 22 through an insulating film 38. ~~Scrapping~~ Strapping word lines 46 for decreasing electric resistance of the word lines are formed on the bit lines 42 through an insulating film 44. The ~~scrapping~~ strapping word lines 46 are connected to the gate electrodes 18 at a certain pitch.

Please replace paragraph the paragraph beginning at page 51, line 10 with the following amended paragraph:

Then, the ~~scrapping~~ strapping word lines 46 are formed on the bit lines 42 through the insulating film 44 (FIG. 27B).

Please replace paragraph the paragraph beginning at page 52, line 15 with the following amended paragraph:

The steps for connecting the word lines with the ~~scrapping~~ strapping word lines are not limited to those used in the present embodiment.